## Abstract

The present invention stacks integrated circuits (ICs) into modules that conserve PWB or other board surface area. In another aspect, the invention provides a lower capacitance memory expansion addressing system and method and preferably with the CSP stacked modules provided herein. In a preferred embodiment in accordance with the invention, a form standard provides a physical form that allows many of the varying package sizes found in the broad family of CSP packages to be used to advantage while employing a standard connective flex circuitry design. In a preferred embodiment, the form standard will be devised of heat transference material such as copper to improve thermal performance. In a preferred embodiment of the memory addressing system, a high speed switching system selects a data line associated with each level of a stacked module to reduce the loading effect upon data signals in memory access.